IN THE SPECIFICATION

Please amend the paragraph beginning on page 8, line 11, as follows:

The counter 130 is initialized by a reset signal RS applied from the control circuit 140 and forwards a final address informing signal ~~FSA~~ FAS to the control circuit 140. The chip address CA is applied to the control circuit 140, while the sector address SA is applied to the register circuit 110 and the core driver 150.

Please amend the paragraph beginning on page 8, line 33, as follows:

The control circuit 140 is further associated with flag generators 141 and 142. Referring to FIG. 9A, the first flag generator 141 makes a signal MULTI informing whether or not the flash memory chips 100 and 200 are configured to a multi-chip package. If the chips are included into the multi-chip package as a single memory system, the signal MULTI is set to "1" by keeping a fuse F1 connected to the power supply voltage VDD (not blown out). Otherwise, if either the chip 100 or 200 is to be utilized as a single chip, the signal MULTI is set to "0" by blowing the fuse F1 out, connecting the signal line to ground through resistor R1.

Please amend the paragraph beginning on page 9, line 9, as follows:

The second flag generator 142, referring to FIG. 9B, makes a signal TOP informing which one of the flash memory chips 100 and 200 assembled in the multi-chip package has the priority in the sequence of the multi-sector erase operation with reference to the address mapping. If the flash memory chip 100 is determined to be the first one to be erased, the signal TOP (i.e., a chip selection signal) is set to "0" by blowing a fuse F2 out (as the case of the present embodiment), connecting the signal line to ground through resistor R2. But, if the flash memory chip 200 is to be determined to be the first one, the chip selection signal TOP may be set to "1" by maintaining the fuse ~~F1~~ F2 without the blowing-out.

Please amend the paragraph beginning on page 17, line 2, as follows:

~~The disclosure is a~~ A semiconductor memory device is operable with a multi-sector erase mode for a multiplicity of memory chips, including a cell array, a register circuit containing information for a sector to be erased, an address clock driving circuit for contemporaneously generating an address clock signal from each memory chips, a counter for generating address signals in sequence, a core driver for executing an erase operation for the sector, and a control circuit thereof.